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(54) **Soft symbol decoding for use in an MLSE-equaliser or convolutional decoder.**

(57)   There is disclosed a soft symbol for use in a decoding process generated from a binary representation of a branch metric. When a hard decision bit is a zero, a preselected number of bits of a binary representation of the branch metric are concatenated with a hard decision bit to form the soft symbol. When the hard decision bit is a one, the ones complement of the preselected number of bits of the binary representation of the branch metric are concatenated with the hard decision bit to form the soft symbol. The concatenation function can be achieved using an exclusive OR function with the preselected bits of the binary representation of the branch metric and the hard decision bit to form the soft symbol. The hard decision bit may be selectable from more than one source.
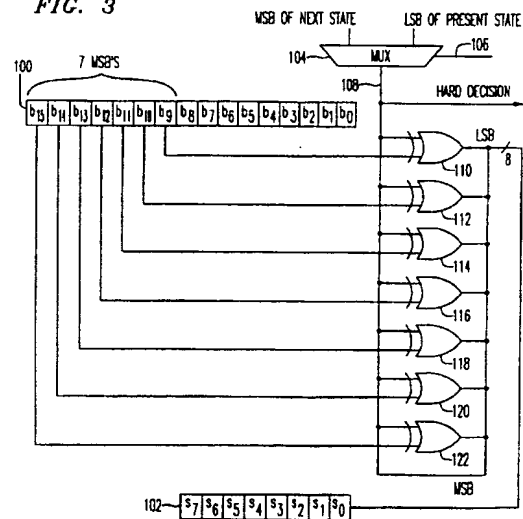
FIG. 3

FIG. 4

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This invention relates generally to the field of digital receivers and particularly to such receivers using soft symbol decoding.

Background of the Invention

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Although telecommunications technology originally developed using copper wires as the transmission media, there is much interest and commercial activity in wireless technology using free space as the transmission media. Wireless technology frees the user from the physical constraint of needing an electrical connection to the transmission media, and is extremely useful to people engaged in activities such as automobile driving.

10   Initial commercial activity developing wireless technology used analog transmission. In the interests of increasing the efficiency of spectrum utilization, digital transmission systems have been developed and it is believed that ultimately a substantial majority of wireless telecommunications will utilize digital transmission systems. Digital systems transmit information as either 0s or 1s. Accurate information transmission depends upon being able to reliably detect transmitted 1s as 1s and 0s as 0s. Accurate detection is not always a simple matter

15 because of factors such as low received signal power and multiple transmission paths caused by reflecting objects between the transmitter and receiver. Error correction techniques have been developed to increase the accuracy of digital communications systems.

     Several techniques that have been developed or utilized to improve the accuracy of the communications system will be briefly described. For example, the information may be convolutionally encoded; this technique

20 reduces the effects of burst channel noise by interleaving the bits of the data stream, that is, the transmitted information. Accuracy of transmission is further improved by the inclusion in the bit stream of redundant bits which are used for error correction in the decoding process. An exemplary error correction scheme uses the Viterbi algorithm; use of the Viterbi algorithm is not limited to convolutional codes. See, Mobile Radio Communications, R. Steele, ed., Chapter 4 Channel Coding by Wong and Hanzo for an exposition of convolutional

25 encoding and the Viterbi algorithm.

     The Viterbi algorithm is a maximum likelihood decoding scheme that provides forward error correction. Each state is represented by a plurality of bits; the number of possible immediately preceding and following states is limited. The permitted transitions from one state to another state are defined as a branch, and a sequence of interconnected branches is called a path. As mentioned, some transitions are not permitted; when

30 the paths resulting from the non-permitted transitions are eliminated, computational efficiency is improved. A branch metric is calculated for each branch and the metric is used to determine which paths survive and which do not survive. One type of decoding is termed hard decision or symbol decoding. In this type of decoding, the decoded symbol is forced to be either a 1 or a 0; that is, the received symbol is quantized into either a 1 or a 0. However, such a two level quantization results in information being lost. This information is retained

35 and utilized in soft symbol or decision decoding. The signal is quantized into a plurality of levels, for example, 4, 8, 16, or more, and given a value which may be positive or negative. The absolute value or magnitude represents the degree of confidence that the signal was accurately received. Decoding now proceeds. The Viterbi decoder selects the branch metric with the largest value and the associated path; it is believed that this represents the most likely path. It is known that soft symbol decoding yields more accurate decoding than does

40 hard symbol decoding.

     A method for soft trellis decoding is described in Unites States Patent 5,144,644 issued on September 1, 1992 to Borth. The method described generates decisions that are based upon other decision making. The degree of confidence in a particular decision is given a relative merit which is related to the difference between the hard and soft symbol values. A transmission system using soft symbol decoding is described in Unites

45 States Patent 4,493,082 issued on January 8, 1985 to Cumberton et al (Cumberton). Cumberton converts five bit words into six bit words by changing the least significant bit of the five bit word into the two least significant bits of the six bit word. These bits are convolutionally encoded and soft decision decoding is used to decide which set of bits was most likely sent.

50 ## Summary of the Invention

     In accordance with the present invention, a soft symbol for use in a decoding process is generated from a binary representation of a branch metric. When a hard decision bit is a zero, a preselected number of bits of a binary representation of the branch metric are concatenated with a hard decision bit to form the soft symbol.

55 When the hard decision bit is a one, the ones complement of the preselected number of bits of the binary representation of the branch metric are concatenated with the hard decision bit to form the soft symbol. The concatenation function can be achieved using an exclusive OR function with the preselected bits of the binary representation of the branch metric and the hard decision bit to form the soft symbol. The hard decision bit

may be selectable from more than one source.

Brief Description of the Drawings

5   Figure 1 is a block diagram of a transceiver;
Figure 2 is a diagram showing an environment in which the invention may be employed;
Figure 3 is a concatenation circuit in which branch metric bits are combined with a hard decision bit to form
a soft symbol; and
Figure 4 is a diagram of the range of soft symbol ones and zeros.

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Detailed Description

Transceiver 10, shown in the block diagram of Figure 1, is a communication system or portion of a com-
munication system such as a mobile digital cellular telephone. Transceiver 10 is comprised of transmitter 12
15   and receiver 14.
A frame, or transmission burst, of transmitted information contains a predetermined number of bits. Each
frame includes starting bits, a first set of information bits, training bits, a second set of information bits, and
ending bits. Typically there are three starting and ending bits, 58 bits in each set of information bits, and 26
training bits for a total of 148 bits per frame. The training bits are known. The starting and ending bits are known
20   and typically are zeroes. Other numbers and distribution of bits are possible depending on the implementation.
In decoding data using the Viterbi process from a series of binary data received at a decoder, the decoder
generates the sequence of data most likely transmitted. The decoder considers all possible state combinations
and produces estimates of signals for all possible state transitions, then compares the estimates with received
data to determine what was the most likely transmitted bit sequence. The initial state of the encoder is known
25   so, therefore, the decoder has a starting point. The end state of the encoder is also known, so the decoder
also has a predetermined ending point. The decoder determines the most likely sequence of state transitions
for the received series of binary data. Each such state represents a symbol instant. At each symbol instant,
there are a number of states that range from 0 up to $2^{C-1}-1$ where C is the constraint length. A typical range
for C would be from 2 to 7. These 2^{C-1} states will be referred to as individual states. A limited number of tran-
30   sitions are possible. At each symbol instant, the accumulated cost is calculated for each of the possible tran-
sitions. The path having an extremum (i.e., minimum or maximum) cost may thereby be determined.
At each symbol instant, each individual state can only progress to a limited number of possible next indi-
vidual states. In addition, each next individual state has only a limited number of possible previous individual
states from which a transition to it can originate.
35   A branch metric is calculated at each symbol instant for each possible transition from all possible individual
states to the next individual state. Various methods for calculating branch metrics are known in the art and will
be detailed below. The branch metric for all branches transitioning to a given next individual state are calcu-
lated, then added to the accumulated cost of the respective originating individual state, resulting in two or more
potential accumulated cost sums. A comparison is made of the various potential accumulated cost sums. An
40   extremum branch metric is selected as the next state accumulated cost. In one embodiment of the invention
the lesser of the cost sums is selected as the next state accumulated cost. (For certain branch metric calcu-
lations, the greater of the cost sums might be selected.) The transition corresponding to the lesser sum is the
more likely transition from the two possible originating individual states to the given next individual state. The
originating individual state of the more likely transition is stored as the surviving origin of a branch to the given
45   next individual state. The lesser sum is the accumulated cost of the next individual state and replaces the ac-
cumulated cost for that individual state stored in traceback RAM 23. This represents the surviving branch to
the next individual state, as is known in the art. This process is repeated for each of the next individual states
and repeated also for each symbol instant until all of the symbols in a burst of bits are decoded.
FIG. 2 is a schematic diagram of a portion of receiver 14 showing a digital signal processor (DSP) 11 having
50   embedded error-correcting co-processor (ECCP) 13 and a DSP core 32. DSP core 32 sets the operational
parameters of the ECCP 13, such as constraint length, and branch metric type, (Euclidean or Manhattan). Core
32 also initiates the Viterbi decoding function of ECCP 13.
Within ECCP 13 is update unit 17, traceback unit 19, and branch metric unit 15. Update unit 17 performs
the add-compare-select operations of the Viterbi process. At every symbol instant there are 2^C state transitions
55   of which 2^{C-1} state transitions survive. The update unit performs the add-compare-select operation and up-
dates 2^{C-1} accumulated cost states in RAM 23. The update unit stores the accumulated cost of each path at
whatever symbol instant is under analysis.
Traceback unit 19 selects a path having the smallest path metric among 2^{C-1} survivor paths at every sym-

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bol instant. The last bit of the path corresponding to the maximum likelihood sequence is delivered to the decoder output. The depth of this last bit is programmable at the symbol rate. If the end state is known, the traceback decoding may be forced in the direction of the correct path by writing the desired end state into a minimum cost index register.

Branch metric unit 15 calculates, for each symbol instant, the branch metric for each possible transition. A variety of metrics have been proposed by those skilled in the art for comparatively evaluating individual branches on the trellis. Viterbi decoders which utilize branch metric units may be capable of performing the Viterbi process utilizing a variety of metrics.

ECCP 13 may be employed to deconvolve signals which have been encoded by a convolutional encoder. In addition, ECCP 13 may be employed to provide maximum likelihood sequence estimation (MLSE) equalization.

In certain applications, ECCP 13 may be required to perform an MLSE process. (In other applications, the ECCP 13 may be required to perform a convolutional decoding as discussed below.) In wide-band width, low data rate applications, additive white gaussian noise (AWGN) is the principal channel impairment and a Euclidean branch metric provided by equation (1) is appropriate for MLSE operation. An Euclidean metric appropriate for MLSE processes is given by

$$BM = (Z_I - E_I)^2 + (Z_Q - E_Q)^2 \quad (1)$$

where

BM = branch metric
Z_I = received in-phase signal component
Z_Q = received quadrature signal component
E_I = estimated received in-phase component for each state transition
E_Q = estimated received quadrature component for each state transition

Consequently, DSP core 32 selects MLSE operation metric unit 25 with an embedded Euclidean branch metric unit. Metric unit 25 performs Euclidean metric calculations on incoming signals as part of an MLSE process.

By contrast, when convolutional decoding is to be performed, either an Euclidean or a Manhattan metric may be appropriate. For example, convolutional decoding over a gaussian channel may require a Euclidean distance measure for rate 1/1 or 1/2 encoding. By contrast, convolutional decoding preceded by MLSE or other linear/non-linear equalization may require a Manhattan distance measure for code rates 1/1 to 1/6. For convolutional decoding with a 1/1 code rate, an Euclidean metric given by equation 2 may be appropriate:

$$BM = (S_O - E_O)^2 \quad (2)$$

where

BM = branch metric
S_O = received signal component
E_O = estimated signal component

For convolutional decoding with a 1/2 code rate, an Euclidean metric given by equation 3 may be appropriate:

$$BM = (S_O - E_O)^2 + (S_I - E_I)^2 \quad (3)$$

where

BM = branch metric
S_O = received first signal component
S_I = received second signal component
E_O, E_I = corresponding estimated signal component associated with each state transition

By contrast, a Manhattan branch metric is provided by equation 4:

$$BM = \sum_{i=1}^{m} |S_i - E_i| \quad (4)$$

for m = 1, 2, 3, 4, 5, 6 depending upon code rate which is 1/m

where

BM = branch metric
S_i = i^{th} received signal
E_i = i^{th} estimated signal

(Note: higher values of m are also permissible). Consequently, when convolutional decoding requiring an Euclidean distance measure is required, metric unit 27 calculates Euclidean metrics. However, should convolutional decoding utilizing a Manhattan metric be required, operation of metric unit 29 is invoked by DSP core

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32 to perform the required metric operation. Whichever metric unit 25, 27 or 29 is selected, it calculates the appropriate metric for each incoming signal. Whichever of the three metric units, 25, 27 or 29, is utilized, the output is provided to multiplexer 30 and then used in the add-compare-select operation performed by update unit 17. Additional metric units may be employed and other metrics such as Hamming may be performed by any of the metric units.

Illustratively, the branch metric unit 15 performs full precision real and complex arithmetic for computing 16 bit branch metrics required for MLSE equalization and/or convolutional decoding. MLSE branch metric unit 25 generates an estimated received complex signal for each symbol instant, n. The received complex signal may be represented by in-phase and quadrature components indicated in equation 5:

$$E(n,k) = EI(n,k) + jEQ(n,k) \quad (5)$$

where

n = symbol instant

$k = 0...2^{C-1}-1$ = all states taking part in Viterbi state transition

C = constraint length

All possible states, $k=0$ to $k = 2^{C-1}-1$, taking part in the Viterbi state transition are convolved with the estimated channel impulse response, H(n), which is provided by equation 6.

$$H(n) = [h(n),h(n-1),h(n-2)...h(n-C+1)]^T \quad (6)$$

where H(n) = estimated channel impulse response

$h(n) = n^{th}$ channel tap

C = constraint length

Each in-phase and quadrature phase part of the channel tap, $h(n) = hI(n) + jhQ(n)$, may be an 8 bit twos complement number (although other representations are acceptable). To simplify data handling, the channel estimates may be normalized prior to loading into ECCP 15 such that the worst case summation of the hI(n) or hQ(n) are confined to be a 10 bit two's complement number (although other representations are possible). In addition, the in-phase and quadrature phase parts of the received complex signal, $Z(n) = ZI(n) + jZQ(n)$ are also confined in a similar manner to be a 10 bit twos complement number. The Euclidean branch metric associated with each of the 2^C state transitions, originally expressed as equation 1, may be rewritten as:

$$BM(n,k) = XI(n,k)^2 + XQ(n,k)^2 \quad (7)$$

where $XI(n,k) = abs \{ZI(n) - EI(n,k)\}$

$XQ(n,k) = abs \{ZQ(n) - EQ(n,k)\}$

where XI, and XQ have an upper saturation limit of OxFF ($= 255_{10}$)

To prevent the occurrence of arbitrarily large branch metrics, the values of XI and XQ are not permitted to exceed OxFF (i.e., 255_{10}). Thus, the absolute value designated in equation 7 is a saturated absolute value having an upper limit of 0xFF. The 16 most significant bits of this 17 bit branch metric are retained for the add-compare-select operation of the Viterbi algorithm in a manner detailed below.

The in-phase and quadrature phase parts of the received complex signal are stored in register bank 31. In addition, the complex estimated channel taps and the generating polynomials may be stored in the same register bank.

As discussed previously, two types of computation are implemented for convolutional decoding. Convolutional decoding over a gaussian channel is supported with an Euclidean metric for rate 1/1 and 1/2 convolutional encoding in unit 27. Convolutional decoding preceded by MLSE equalization or other linear/non-linear equalization is supported with a Manhattan distance measure for rates 1/1 through 1/6 convolutional encoding in unit 29.

The branch metric corresponding to the surviving transition can be converted into a binary soft symbol. Figure 3 shows a circuit to convert a multiple bit branch metric directly into a soft symbol. Branch metric 100 is a multiple bit word. In the exemplary embodiment branch metric 100 has 16 bits of which the seven most significant bits used to generate a soft symbol 102. The invention is not limited to a 16 bit branch metric, employing the most significant bits to generate a soft symbol, or generating a soft symbol from seven bits.

In the exemplary embodiment, either the most significant bit of the next state, or the least significant bit of the present state may be used in generating a soft symbol as shown in Figure 3. The most significant bit of the next state and the least significant bit of the present state are provided as inputs to multiplexer 104. Multiplexer 104 is responsive to select input 106 to selectively pass one of the signals appearing at the input to its output 108. The output 108 of multiplexer 104 provides a first input to each of exclusive OR (XOR) gates 110 through 122. The output 108 can alternatively be used as a hard decision. While exclusive OR gates are shown in the exemplary embodiment, it is recognized that combinatorial logic could provide the same function. The second input to each of XOR gates 110 through 122 is provided by a preselected number of the most significant bits of branch metric 100. In the exemplary embodiment shown in Figure 3, the preselected number of bits is seven, and the preselected bits are the most significant bits, though the invention is not limited thereto.

The most significant bit of branch metric 100 provides the second input to XOR 122. The least significant of the preselected number of most significant bits of branch metric 100 provides the second input to XOR 110. Output 108 from multiplexer 104 is concatenated as the most significant bit of the binary soft symbol 102. The second most significant bit of soft symbol 102 is the output of XOR 122. The least significant bit of soft symbol 102 is the output of XOR 110.

Operation of the circuit of Figure 3 and conversion of a branch metric to a binary soft symbol is further understood in conjunction with Figure 4. The concatenated bits forming soft symbol 102 have a range that extends from 00000000_2 (0_{10}) to 11111111_2 (255_{10}). The range of soft symbol 102 representing a zero 00000000_2 (0_{10}), the best zero, to 01111111_2 (127_{10}), the worst case zero. The range of soft symbol 102 representing a one extends from 10000000_2 (128_{10}), the worst case one, to 11111111_2 (255_{10}), the best case one.

Output 108 determines whether a soft symbol represents a soft zero or a soft one. The hard decision bit positions the soft symbol on the appropriate side of the transition from a zero to one. The boundary between a zero and a one is determined by the most significant bit of the soft symbol.

When output 108 is a zero, the output of each XOR 110 through 122 is the same as the bit of branch metric 100 received at the second input of each exclusive or gate. In this manner, soft symbol 102 is constructed with output 108 as the most significant bit, concatenated with the preselected number of most significant bits of branch metric 100, here seven.

When output 108 is a one, the output of each XOR 110 through 122 is the ones complement of the bit of branch metric 100 received at the second input of each exclusive or gate. In this manner, soft symbol 102 is constructed with output 108 as the most significant bit, concatenated with ones complement of the most significant bits of branch metric 100. The ones complement reflects the confidence level information across the line of demarcation between a zero and a one.

A soft symbol generated in accordance with the present invention does not include any negative numbers in the range of soft symbol zeros and ones and therefore does not require any twos complement binary representations. Soft symbols generated in accordance with the present invention can be used in subsequent signal processing to obtain higher performance. Soft decision decoding improves the coding gain of the overall system in which soft symbol decoding is employed.

The invention is particularly useful in communication systems and equipment employing integrated circuits including this technique. Such communications systems and equipment have the advantage of reduced complexity of circuitry to accomplish the signal processing. Soft symbols in accordance with the present invention do not require twos complement arithmetic.

While the illustrative embodiment of the invention has not been described as incorporating pipelining, one skilled in the art would recognize the enhanced computational efficiency available by utilizing pipelining in the design. Pipelining is achieved by initiating computation with a new data set before completing computations with a previous set of data. The more latches used in pipelining, the greater the depth of pipelining. Pipelining causes an initial latency in computation time required to fill the pipeline, but maximizes usage of resources such as adders and subtractors.

Claims

1. A method of generating a soft symbol for use in decoding a received digital signal into bits that are ones and zeroes, the soft symbol being generated from bits of a binary representation of a branch metric, the method including the steps of generating a hard decision bit (e.g., 108) associated with a state, CHARCTERIZED BY

    concatenating(e.g., 110, 112, 114, 116, 118, 120, 122) a preselected number of said bits of a binary representation of the branch metric (e.g., 100) with the hard decision bit (e.g., 108) to form the soft symbol (e.g., 102) when the hard decision bit (e.g., 108) is a first value; and

    concatenating(e.g., 110, 112, 114, 116, 118, 120, 122) the ones complement of a preselected number of bits of a binary representation of the branch metric (e.g., 100) with the hard decision bit (e.g., 108) to form the soft symbol (e.g., 102) when the hard decision bit (e.g., 108) is not the first value.

2. A method as recited in claim 1, wherein the step of concatenating a preselected number of said bits of a binary representation of the branch metric with the hard decision bit to form the soft symbol when the hard decision bit is a first value, is further CHARACTERIZED BY

    selecting the preselected number of bits as the most significant bits of the binary representation of the branch metric (e.g., 100).

3. A method of generating a soft symbol for use in decoding a received digital signal into bits that are ones and zeroes, the soft symbol being generated from bits of a binary representation of a branch metric, the method including the steps of generating a hard decision bit (e.g., 108) associated with a state, CHARACTERIZED BY

concatenating (e.g., 110, 112, 114, 116, 118, 120, 122) the ones complement of a preselected number of bits of a binary representation of the branch metric (e.g., 100) with the hard decision bit (e.g., 108) to form the soft symbol (e.g., 102) when the hard decision bit is a one; and

concatenating (e.g., 110, 112, 114, 116, 118, 120, 122) a preselected number of bits of a binary representation of the branch metric (e.g., 100) with a hard decision bit (e.g., 108) to form the soft symbol (e.g., 102) when the hard decision bit is not one.

4. A method as recited in claim 1 or 3, wherein the step of concatenating the ones complement of a preselected number of bits of a binary representation of the branch metric with a hard decision bit to form the soft symbol when the hard decision bit is a one, further CHARACTERIZED BY

selecting the preselected number of bits as the most significant bits of the binary representation of the branch metric (e.g., 100).

5. A circuit for generating a binary soft symbol for use in a decoding received digital signal into bits that are ones and zeroes, the circuit including means (e.g., 104) for receiving a hard decision bit (e.g., 108), the hard decision bit (e.g., 108) associated with a state and means for storing a binary representation of a branch metric associated with the state, CHARACTERIZED BY

a plurality of exclusive OR gates (e.g., 110, 112, 114, 116, 118, 120, 122) corresponding in number to a predetermined number of bits of the binary representation of the branch metric associated with the state, each of the plurality of exclusive OR gates having a first input to receive a bit of the binary representation of the branch metric (e.g., 100), a second input to receive the hard decision bit (e.g., 108), and an output, the output of the plurality of exclusive OR gates (e.g., 110, 112, 114, 116, 118, 120, 122) collectively providing the least significant bits of a soft symbol (e.g., 102); and

means for providing the hard decision bit (e.g., 108) as the most significant bit of the soft symbol (e.g., 102), whereby a preselected number of bits of the binary representation of the branch metric are exclusively ORed with the hard decision bit to generate a soft symbol from a branch metric.

6. A circuit as recited in claim 5 further CHARACTERIZED BY the means for receiving a hard decision bit is a multiplexer (e.g., 104), the multiplexer (e.g., 104) capable of selecting a hard decision bit from one of at least two sources.

7. A receiver (e.g., 10) for decoding a sequence of received symbols into bits that are ones and zeroes using soft symbol decoding, including means (e.g., 14) for receiving a sequence of symbols transmitted over a transmission channel, means (e.g., 15) responsive to the means for receiving (e.g., 14) for calculating a branch metric (e.g., 100) for a possible transition from an individual state at one symbol instant to an individual state at a next symbol instant, the branch metric (e.g., 100) having a binary representation, and means (e.g., 104) for receiving a hard decision bit (e.g., 108) associated with one of said symbol instants, CHARACTERIZED BY

a plurality of exclusive OR gates (e.g., 110, 112, 114, 116, 118, 120, 122) corresponding in number to a predetermined number of bits of the binary representation of the branch metric (e.g., 100) associated with the next symbol instant, each of the plurality of exclusive OR gates (e.g., 110, 112, 114, 116, 118, 120, 122) having a first input to receive a bit of the binary representation of the branch metric, a second input to receive the hard decision bit (e.g., 108), and an output, the output of the plurality of exclusive OR gates collectively providing the least significant bits of a soft symbol (e.g., 102); and

means for providing the hard decision bit (e.g., 108) as the most significant bit of the soft symbol (e.g., 102), whereby a soft symbol is generated from a branch metric for use in the decoding.

8. A receiver as recited in Claim 5 or 7, further CHARACTERIZED BY the predetermined number of bits are selected as the most significant bits of the binary representation of the branch metric (e.g., 100).

9. A receiver as recited in claim 5 or 7, wherein the predetermined number of bits of the binary representation of the branch metric (e.g., 100) used in generating the soft symbol (e.g., 102) is one less than the number of bits in the soft symbol (e.g., 102).

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10. A receiver as recited in claim 9, further CHARACTERIZED BY the predetermined number of bits is seven.

11. A receiver as recited in claim 10, further CHARACTERIZED BY the means for receiving a hard decision bit is a multiplexer (e.g., 104), the multiplexer (e.g., 104) capable of selecting a hard decision bit (e.g., 108) from one of at least two sources.

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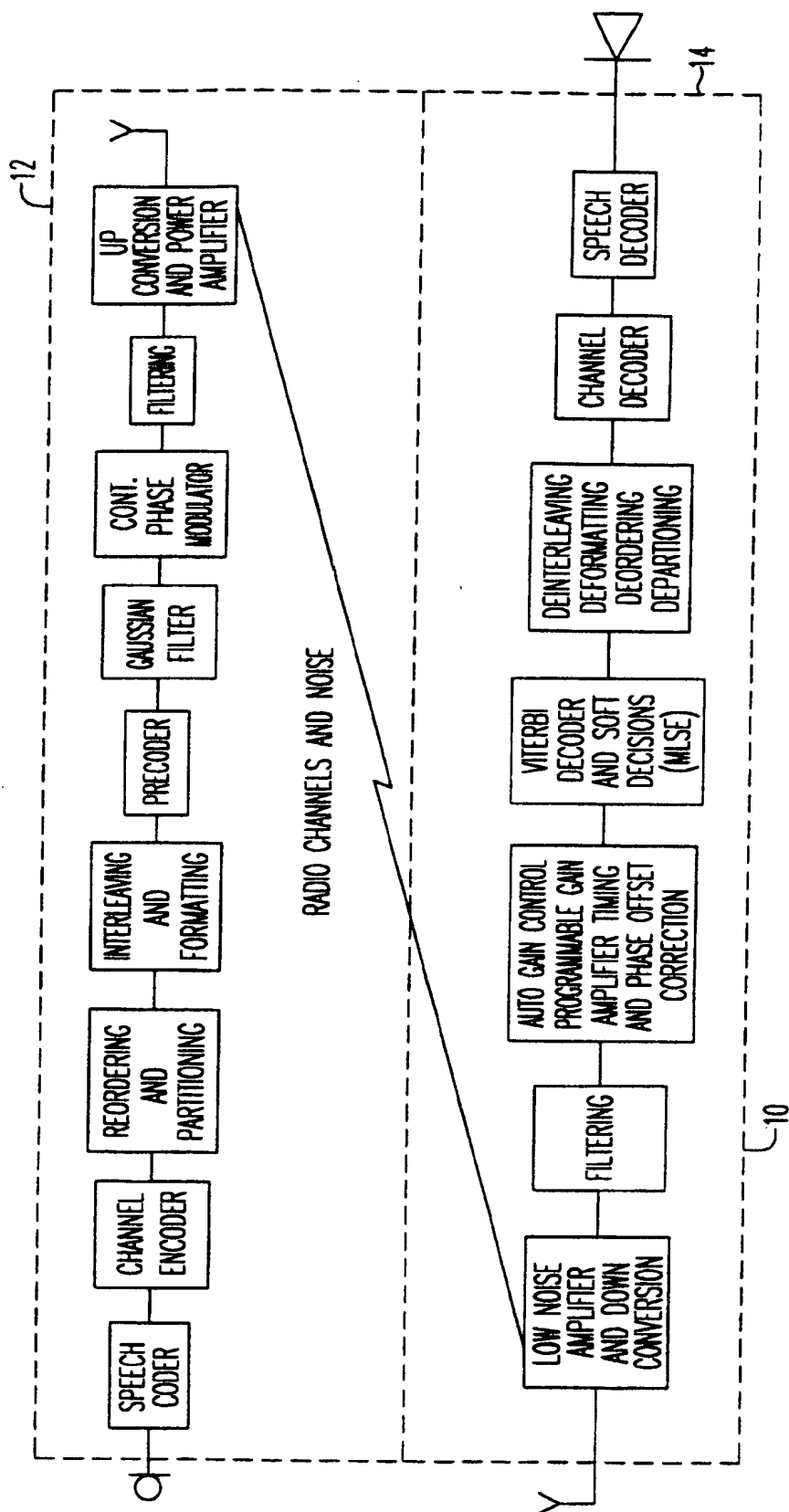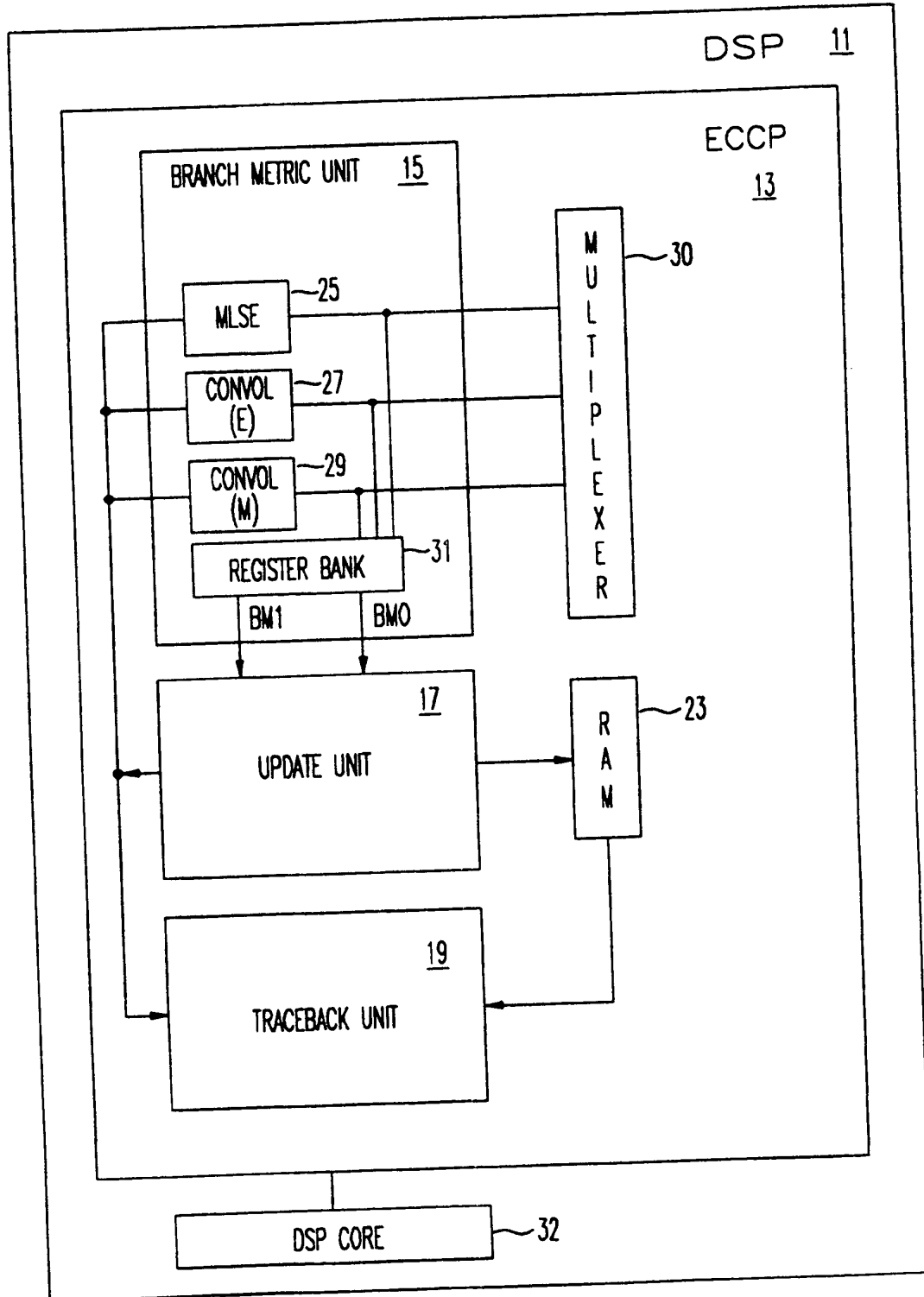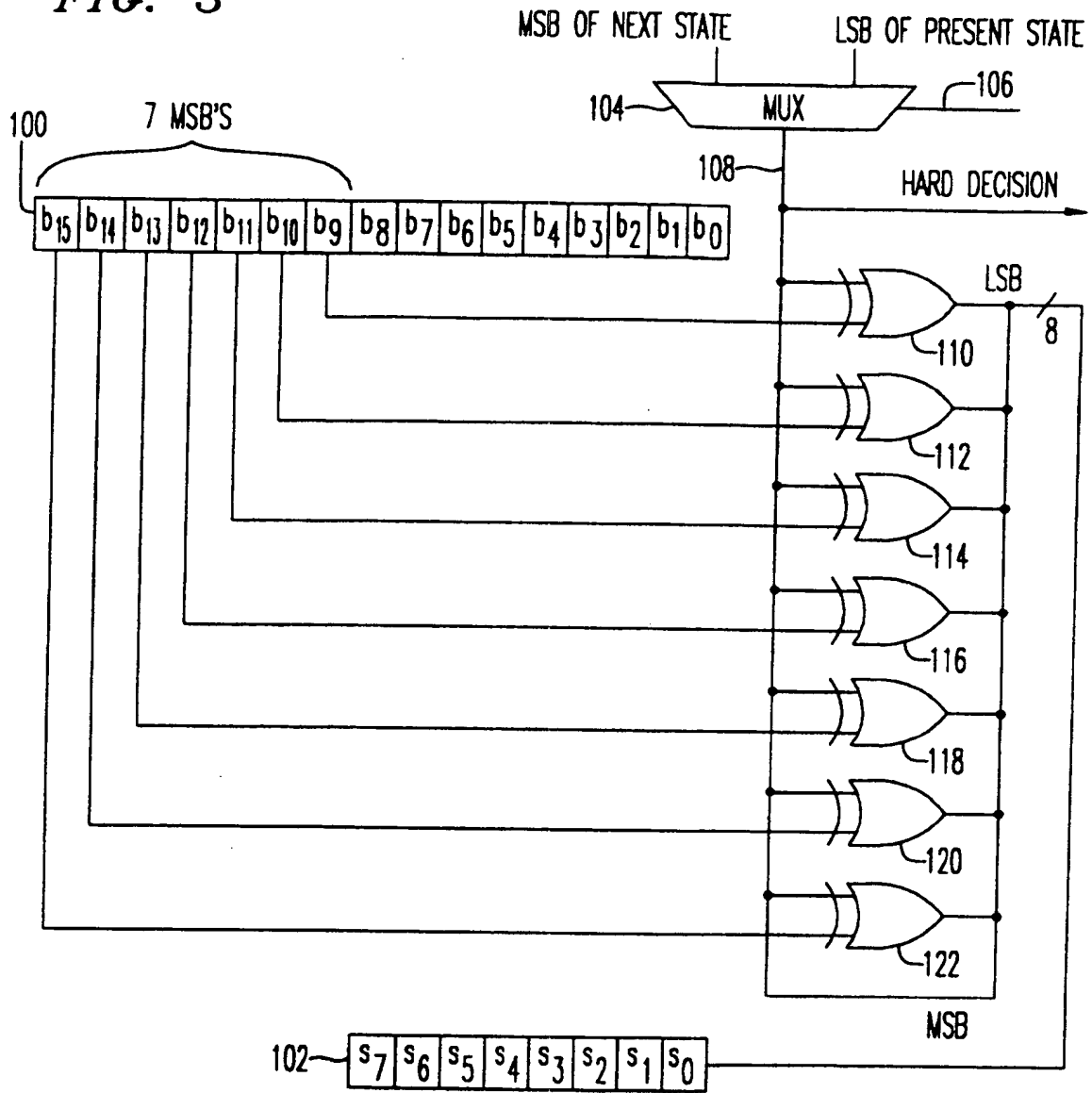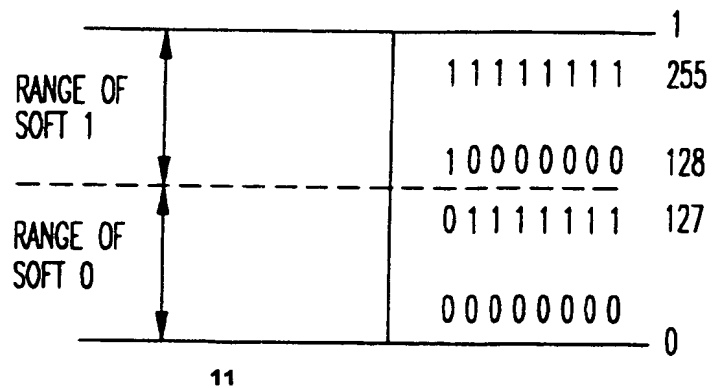25

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FIG. 1

RADIO CHANNELS AND NOISE

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FIG. 2

FIG. 3

MSB OF NEXT STATE   LSB OF PRESENT STATE

104 — MUX — 106

108 —

HARD DECISION

100   7 MSB'S

| b_{15} | b_{14} | b_{13} | b_{12} | b_{11} | b_{10} | b_9 | b_8 | b_7 | b_6 | b_5 | b_4 | b_3 | b_2 | b_1 | b_0 |

LSB

110
8

112

114

116

118

120

122

MSB

102 — | s_7 | s_6 | s_5 | s_4 | s_3 | s_2 | s_1 | s_0 |

FIG. 4

		1
RANGE OF SOFT 1	1 1 1 1 1 1 1 1	255
	1 0 0 0 0 0 0 0	128
RANGE OF SOFT 0	0 1 1 1 1 1 1 1	127
	0 0 0 0 0 0 0 0	0

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European Patent Office	**EUROPEAN SEARCH REPORT**	Application Number EP 95 30 1278

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
D,A	WO-A-91 06165 (MOTOROLA INC.) * abstract * * page 2, line 29 - page 3, line 28 * * page 5, line 5 - page 7, line 16 * ---	1-11	H03M13/00 H04L1/00 H04L25/03
A	DE-A-42 24 214 (DEUTSCHE FORSCHUNGSANSTALT FÜR LUFT- UND RAUMFAHRT E.V.) * abstract * * page 2, line 30 - line 38 * * page 2, line 45 - line 54 * * page 7, line 10 - line 13 * * figures * ---	1-11	
A	EP-A-0 391 354 (DEUTSCHE FORSCHUNGSANSTALT FÜR LUFT- UND RAUMFAHRT E.V.) * page 2, line 50 - page 3, line 26 * * page 3, line 54 - page 4, line 31 * ---	1-11	
A	IEEE INTERNATIONAL CONFERENCE ON COMMUNICATIONS ICC '93, GENEVA, CH, 23.-26.05.93, vol.2, 23 May 1993, IEEE, NEW YORK, US pages 741 - 745, XP371183 N. SESHADRI / P. HOEHER: 'On Post-Decision Symbol-Reliability Generation.' * page 741, right column, paragraph 1 - page 742, left column, paragraph 2 * * page 744, left column, paragraph 1 * * page 744, right column, last paragraph - page 745, left column, last paragraph * ---	1-11	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H03M H04L
D,A	EP-A-0 052 463 (PLESSEY OVERSEAS LTD.) * page 5, line 1 - page 6, line 3; figure 2 * * page 11, line 5 - line 21; figure 11 * -----	1-11	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	21 June 1995	Gries, T

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